640×512/15μm InGaAs SWIR FPA detector Manual

（SWF640-ACME、VISF640-ACME）

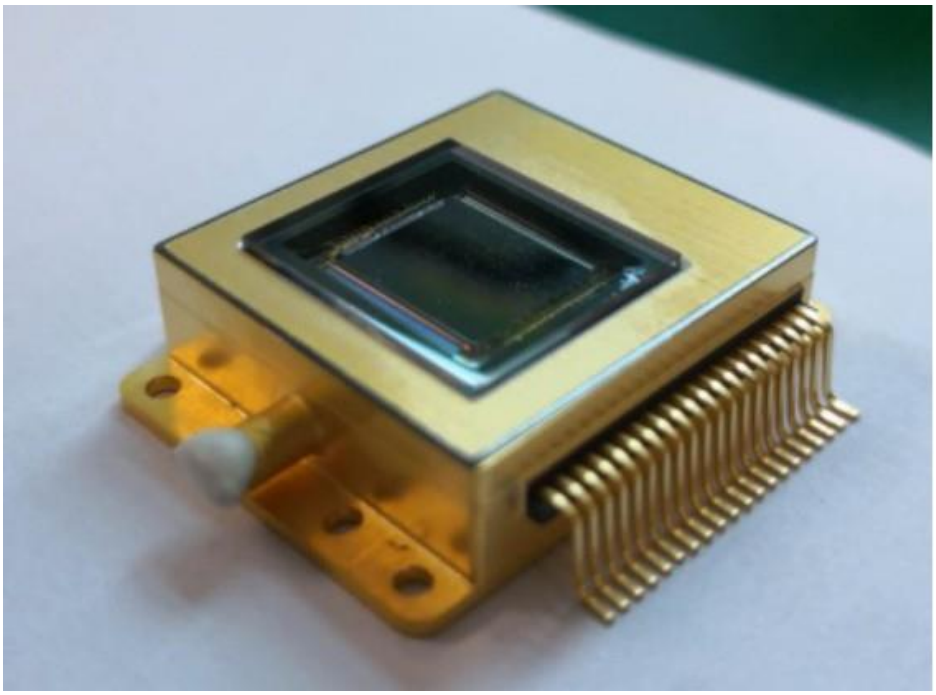
version 4.3

FEATURES

1. Shortwave infrared (0.9μm~1.7μm，can be extended to visible light) InGaAs focal plane array detector；
2. 640(H)×512(V) pixel array specifications；
3. 15μm×15μm pixel spacing；
4. 20×2 pin metal vacuum package；
5. 2/4/8 analog video output；
6. Built-in temperature sensor，Built-in TEC cooler；
7. Pixel operable rate >99.5%；
8. Quantum efficiency >70%。

APPLICATIONS

1. Shortwave infrared imaging
2. Spectral imaging
3. Surveillance (night vision)
4. Semiconductor inspection
5. Medicine and Biology
6. Optical fiber communication
7. Astronomy science
8. High temperature imaging
9. Environmental and resource monitoring



Summary

InGaAs 640×512/15 μm focal plane array (FPA) detector, which has the characteristics of high detection sensitivity, long service life, low power consumption and light weight, provides 2/4/8 analog video output, and the maximum frame rate is over 300 Hz; The response bandwidth is 0.9μm(0.4μm can be extend) ~ 1.7μm.

The product is vacuum packaged in a metal tube shell, with a tube leg spacing of 1mm, a built-in temperature sensor and a 2 stage TEC cooler, the operating temperature range covers −40°C to +70°C, and the weight is less than 20g.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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1. Main technical parameters

technical parameter	value		
pixel size	15μm × 15μm		
spectral response	0.9μm(0.4μm can be extend) -1.7μm		
Photosensitive pixel area	9.6mm(H) × 7.68mm(V)		
Packaging form	40-pin Metal vacuum package		
overall dimension	32mm ×23.5 mm ×7.2 mm		
Pixel operability	≥99.5%		
quantum efficiency	≥ 70%		
Charge conversion gain	HG: 106μV/e-(1.5f)	MG: 20μV/e-(8fF)	LG: 0.82μV/e- (196fF)
Analog output range	1.8V (Design value)		
Integration/readout mode	Snapshot，Integration Then Read(ITR)，Integration While Read(IWR)，CDs mode, etc		
Frame rate	Max value≥300 Hz @ 8 channels		
Windowing	Programmable ≥4×8(2-Channel output mode)；≥4×16(4-Channel output mode)；≥4×32(8-Channel output mode)		
power supply	3.3V/3.6V Analog Core, Digital I/O,1.8V Digital Core		
operation temperature	−40°C to +70°C		
Temperature sensor coefficient	Gain:-6.0mV / K VTEMP=2.136V@27°C		
Non-uniformity	<4%		
weight	≤20g		
Refrigeration mode	2 stage TEC cooler		
Window material	sapphire		

Typical test conditions: **A**mbient temperature: 23 ℃.

2. Block diagram of readout circuit system

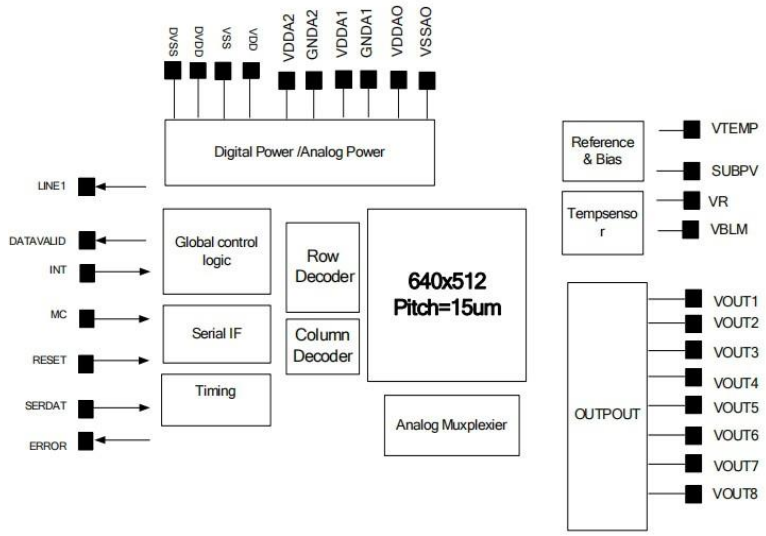


Figure 1. Block diagram of readout circuit system

3. PIN definition and function description

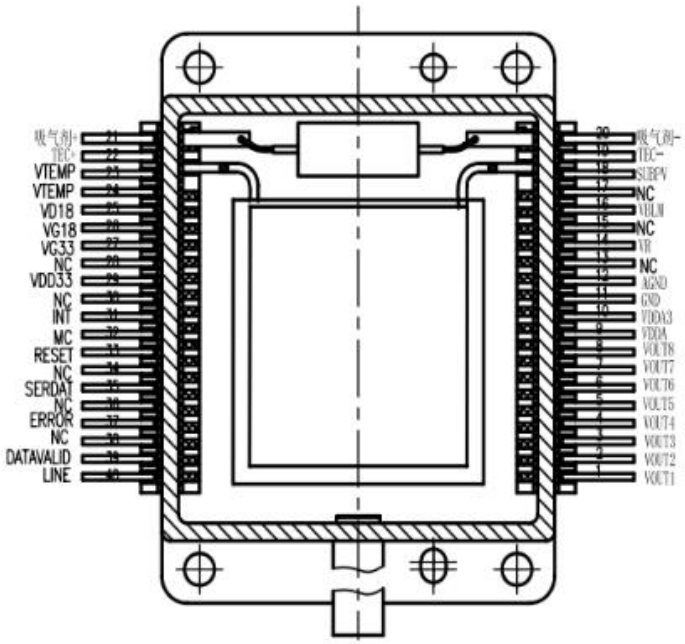


Figure 2. InGaAs640x512 pin definition

Table 1. InGaAs 640x512/15μm Pin definition description

Pin No.	**name**	describe
1	OUT1	Third channel analog output of 8 channels and 4 channels and 2 channels
2	OUT2	The 4th channel analog output of 8 channels and 4 channels and 2 channels
3	OUT3	Third channel analog output of 8 channels and 4 channels
4	OUT4	The 4th channel analog output of 8 channels and 4 channels
5	VOUT5	The 5th analog output of 8 channels
6	VOUT6	The 6th analog output of 8 channels
7	VOUT7	The 7th analog output of 8 channels
8	VOUT8	The 8th analog output of 8 channels
9	VDDA	Analog power supply (3.6V)
10	VDDA3	Analog IO power supply (3.6V)
11	GND	Analog ground
12	AGND	Analog ground
13	NC	Hang in the air
14	VR	Bias voltage input (3.3V)
15	NC	Hang in the air
16	VBLM	Bias voltage (support external adjustable)
17	NC	Hang in the air
18	SUBPV	Detector common terminal (N terminal)，external input 2.7V～3.2V
19	TEC-	TEC Cooler-
20	Getter-	Getter electrode-
21	Getter+	Getter electrode+
22	TEC+	TEC Cooler+
23	VTEMP	Built-in temperature sensor output voltage
24	VTEMP	Built-in temperature sensor output voltage
25	VD18	Digital core power supply (1.8V)
26	VG18	Digital core ground
27	VG33	Digital IO ground
28	NC	Hang in the air
29	VDD33	DigitalIOpower supply (3.3V)
30	NC	Hang in the air
31	INT	System frame synchronization signal
32	MC	System master clock (Master Clock)
33	RESET	External reset signal (active high)
34	NC	Hang in the air
35	SERDAT	Serial data input
36	NC	Hang in the air
37	ERROR	Serial output check
38	NC	Hang in the air
39	DATAVALID	Valid data output mark signal
40	LINE1	The first line of data output mark signal

4. Input and output interface configuration

4.1 Bias

Table 2. List of analog of bias voltage configuration

Port name	Operating voltage range	Default voltage value	Drive current	Input noise requirements (rms)
VR	External input 3V~3.3V	3.3V	>60mA	Less than ± 0.05mV (10Hz~18MHz)
VBLM	Internally generated, supporting external adjustment (0V~2.0V)	1.0V	>5mA	Less than± 0.05mV (10Hz~18MHz)
SUBPV	External input 3.1V~3.5V	3.2-3.3V	>5mA	Less than± 0.05mV (10Hz~18MHz)

4.2 Power supply configuration

Table 3 Power supply voltage configuration list

Port name	purpose	Operating Voltage	Typical value	Drive current	Noise requirements (RMS)
VDDA3	Analog power supply	3.3V~3.8V	3.6V	>80mA	Less than 1mV(1K~12MH)
VDDA	Logic and analog power supply	3.3V~3.8V	3.6V	>150mA	Less than 10mV(10Hz~22MHz)
VD18	Digital power supply	1.62V~1.98V	1.8V	>30mA	Less than 20mV(1K~22MHz)
VD33	Digital IO power supply	3.0V~3.3V	3.3V	>20mA	Less than 10mV(1K~22MHz)

4.3 Clock

Table 4. Input clock configuration list

Port name	Clock frequency range	VH/VL	Rise/fall time
INT	<100Hz	3.3V/0V	<50ns
MC	2MHz～18MHz	3.3V/0V	<6ns
SERDAT	2MHz～18MHz	3.3V/0V	<6ns

4.4 Serial port register configuration

Table 5 Serial port register configuration settings

Data serial number	name	Features	Number of digits	Default value
1～4	START[3:0]	Serial port enable control bit	4bit	4'b1101
5～6	GAIN[1:0]	Integral gain control	2bit	2'b00
7	UPCOL	Image flip and mirror	1bit	1'b1
8	UPROW		1bit	1'b1
9	SIZEA	Window format	1bit	1'b1
10	SIZEB		1bit	1'b1
11～19	Cmin[8:0]	Coordinates of the start and end positions of the window	9bit	9'b0
20～28	Cmax[8:0]		9bit	9'b0
29～37	Cmin[8:0]		9bit	9'b0
38～46	Cmax[8:0]		9bit	9'b0
47～48	PWCTL[1:0]	Global power consumption control bit	2bit	2'b01
49～50	NBOUT[1:0]	NC positioning of output channel	2bit	1'b11
51～53	ICTL_AWP[2:0]	Pixel power consumption control bit	3bit	3'b010
54～55	ICTL_BUF[1:0]	Column BUF power consumption control bit	2bit	2'b01
56～57	ICTL_AK[1:0]	Driving signal establishment time control bit	2bit	2'b01
58	ICTL_OUT	Output BUF power control bit	1bit	1'b0
59～61	T_READY[2:0]	Integral preparation time control bit	3bit	3'b101
62	BLM_EN	Anti halo enable control bit	1bit	1'b1
63～65	BLM_CTL[2:0]	Anti corona voltage configuration bit	3bit	3'b010
66	T_CSH	Sampling signal CSH control bit	1bit	1'b0
67～68	T_RSW[1:0]	Test mode control bit	2bit	2'b10
69～70	T_SH[1:0]	Test mode control bit	2bit	2'b10
71～74	TCDS[3:0]	CDS sampling time control bit	4bit	4'b0111
75	T_TS2	Test mode control bit	1bit	1'b0
76	CDS_MODE	CDS mode control bit	1bit	1'b1
77	NDRO	NDRO mode control bit	1bit	1'b0
78	IMRO	IMRO mode control bit	1bit	1'b0
79	BWL	Bandwidth limiting control bit	1bit	1'b1
80	T_ROW_EN	Test mode control bit	1bit	1'b0
81	TOS_EN	Test mode control bit	1bit	1'b0
82～83	T_TD5[1:0]	Test mode control bit	2bit	1'b10
84～85	T_WAIT[1:0]	Test mode control bit	2bit	1'b00
86	T_DYMPWR_ENB	Test mode control bit	1bit	1'b0
87	LT_EN	Test mode control bit	1bit	1'b0
88	ATEST_VN	Test mode control bit	1bit	1'b0
89～92	ATEST_OE[3:0]	Test mode control bit	4bit	4'b0000
93	DTEST_EN	Test mode control bit	1bit	1'b0
94～95	DTEST[1:0]	Test mode control bit	2bit	2'b00
96～103	TEST_A[7:0]	Test mode control bit	8bit	8'b0000,0000

Note：for example：Represents the default value of 1-4 bit data sequence number 4'b1101，from low to high (1-4) are 1, 1, 0, 1.

The status table of control bits 5-103 is described as follows.

Integral capacitor size control bit --GAIN[1:0]

GAIN[1]	GAIN[0]	Gain configuration
0	0	High gain (default)
0	1	Mid range gain
1	X	Low gain

Control model

IMRO mode control ----- IMRO(multiple integral readout)-----priority Higher than NDRO, CDS mode

NDRO mode control ----- NDRO(Nondestructive readout)---- Priority higher than CDS mode

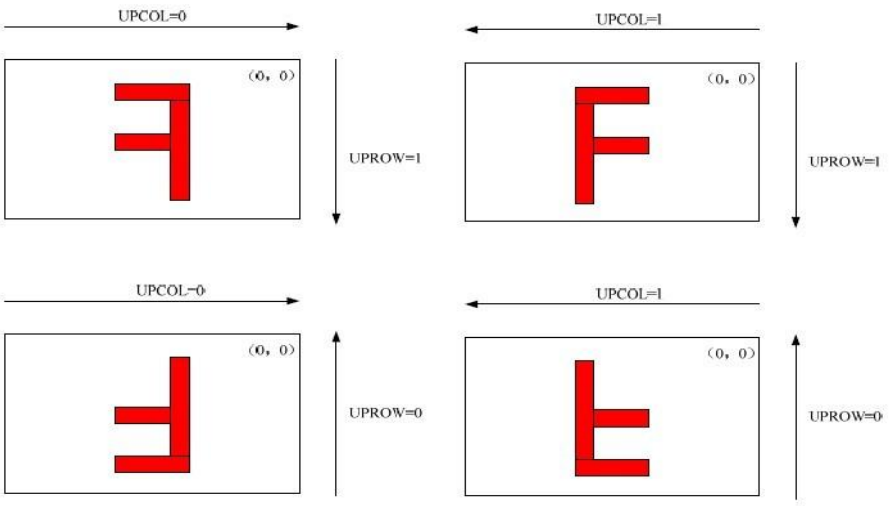
CDS mode control ----- CDS_MODE---- GAIN[1] Priority higher than CDS_MODE

IMRO	NDRO	GAIN[1]	CND_MODE	Readout mode
0	0	0	1	CDS mode (default)
0	0	0	0	Non CDs mode
0	0	1	x	Non CDs mode
0	1	0	0	(in non CDs mode)NDRO mode
1	1	0	1	(in non CDs mode)NDRO mode
1	1	1	x	(in non CDs mode)NDRO mode
1	x	0	0	(in non CDs mode) IMRO mode
1	x	0	1	(in non CDs mode) IMRO mode
1	x	1	x	(in non CDs mode) IMRO mode

Note 1: In the process of switching from "CDs mode" to "non CDs mode", it is recommended that users switch to "non CDs mode" first, and then switch to "normal non CDs mode".

Image flipping and mirroring--UPCOL，UPROW

UPCOL	UPROW	Image output sequence
1	1	Right to left, top to bottom (default)
1	0	From right to left, from bottom to top
0	1	From left to right, from top to bottom
0	0	From left to right, from bottom to top



Schematic diagram of image flipping and mirroring

Fixed format and window configuration --SIZEA，SIZEB，RMAXCMIN、CMAX、RMIN、RMAX

SIZEA	SIZEB	Window format
1	1	640×512(default)
1	0	640×480
0	1	512×512
0	0	Custom window

Constraints of custom windows

1） Window row number configuration bit：Rmin, Rmax 9 bit each

RA=RMIN, 0≤RMIN≤508 RB=RMAX, RMIN+3≤RMAX≤511

The minimum number of rows is 4；

2） Window column number configuration bit ：

Window column configuration bits: Cmin, Cmax, 9 bit each

——Eight channel mode：(NBOUT[1:0]=2b’11default)

CA=8×CMIN, 0 ≤CMIN≤78

CB=8×CMAX+7, CMIN+1≤CMAX≤79

The minimum window format is 16 (columns)×4 (lines)

——Four channel mode：(NBOUT[1:0]=2b’10)

CA=4×CMIN, 0 ≤CMIN≤158

CB=4×CMAX+3, CMIN+1≤CMAX≤159

The minimum window format is 8 (columns)×4 (lines)

——Two channel mode：（NBOUT[1:0]=2b'0x）

CA=2×CMIN, 0 ≤CMIN≤318

CB=2×CMAX+1, CMIN+1≤CMAX≤319

The minimum window format is 4 (columns)×4 (lines)

Power consumption control --PWCTL[1:0]

PWCTL[1]	PWCTL[0]	Power consumption ratio
0	0	50%
0	1	100%(default)
1	0	150%
1	1	200%

Output channel number control --- NBOUT[1:0]

NBOUT[1]	NBOUT[0]	state
0	x	Two channels
1	0	Four channels
1	1	Eight channels

Pixel power consumption control --ICTL_AWP[2:0]

ICTL_AWP[2]	ICTL_AWP[1]	ICTL_AWP[0]	**Pixel power consumption**
0	**0**	**0**	**33%**
0	**0**	**1**	**67%**
0	**1**	**0**	100%（default）
0	**1**	**1**	133%
1	**0**	**0**	167%
1	**0**	**1**	200%
1	**1**	**0**	233%
1	**1**	**1**	267%

Column BUF power consumption control --ICTL_BUF[1:0]

ICTL_BUF [1]	**ICTL_BUF** [0]	Power consumption ratio
0	0	50%
0	1	100%(default)
1	0	150%
1	1	200%

Drive signal setup time control --ICTL_AK[1:0]

ICTL_AK[1]	ICTL_AK[0]	Control signal rising / falling edge time
0	0	1.5us
0	1	0.8us(default)
1	0	0.5us

1	1	< 350ns

Output BUF power consumption control --ICTL_OUT

ICTL_OUT	Power consumption ratio
0	100%（default）
1	131%

Integral preparation time control --T_READY[2:0]

T_READY[2]	T_READY [1]	T_READY [0]	Control signal rising / falling edge time
0	0	0	100us
0	0	1	50us
0	1	0	20us
0	1	1	4us
1	0	0	2us
1	0	1	1us（default）
1	1	0	0.5us
1	1	1	120ns

Note: INT high level width (i.e. integration time) should be greater than integration preparation time. To achieve the shortest integration, configure t_ READY[]=3b’111。In CDS mode, the integration time needs to be greater than t_ Ready time + TCDS time.

Anti halo function control --BLM_EN and BLM_CTL[2:0]

BLM_EN	BLM_CTL[2:0]	VBLM Voltage value
0	X	0V
1	000	0.80V
1	0001	0.93V
1	011	1.07V
1	100	1.15V
1	101	1.21V
1	110	1.28V
1	111	1.35V

TCDS clock number control signal --TCDS

TCDS	TCDS Number of clocks
0000	0Tmc
0001	36Tmc
0010	108Tmc
0011	180Tmc
0100	252Tmc

0101	324Tmc
0110	396Tmc
0111	468Tmc (default)
1000	540Tmc
1001	612Tmc
1010	684Tmc
1011	756Tmc
1100	828Tmc
1101	900Tmc
1110	972Tmc
1111	1044Tmc

Note: in CDS mode, the integration time must be greater than the time configuration of TCDS.

Bandwidth limit control --BWL

BWL	Bandwidth limiting function
0	No width limit
1	Bandwidth limitation(default)

Short integral application configuration method -- CDS_ Mode and T_ Ready combination：

When CDS_MODE=low, T_Ready = 3'b111, the circuit enters the non CDS mode, and the circuit supports the configuration with the shortest integration time greater than 3Tmc. Application scenarios are suitable for applications with short exposure time, such as active illumination gated imaging.

4.5 constraint

1) Analog output signal：VOUT1～VOUT8

Load requirements per port：Cload<25pF, Rload>100Kohm

2) Logic output signal： DATAVALID, LINE1, ERROR, EOC

Output level range： VOH=VDD-0.3V～VDD, VOL=0～0.3VOutput load：Cload<15pF

3) Analog power supply 1：VDDA3

It is required to supply a low-noise power supply from outside, which is connected to the chip after filtering.Configuration requirements: After external

resistance of 2~5 ohms, 22uF//0.1uF capacitors are connected to the analog ground to form an R-C filter, which is then used as the power input of the chip VDDA3.

4) Analog power supply 2：VDDA

When the external power supply is required to be connected to the Pin, a bypass capacitor greater than 10μF / / 0.1μF is used for filtering.

5) Digital power supply：VDD, VDD33

When the external power supply is required to be connected to the Pin, a bypass capacitor larger than 4.7μF / / 0.1μF is used for filtering.

6) Temperature sensor output：VTEMP

The output end of VTEMP is externally connected with 20kohm and 10uF to form R-C filtering, and then used for external ADC

7) Detection.Bias voltage：VR

An external low-noise power supply is required. When connecting to the Pin, first pass a bypass capacitor larger than 1μF//0.1μF for filtering.

5. The introduction of processing circuit

The detector circuit consists of pixel array, column sample and hold circuit, column buffer circuit, channel output buffer circuit, timing control and serial port logic circuit. The chip can work at room temperature and low temperature.

The processing circuit adopts snapshot working mode, supports non-destructive readout (NDRO) working mode; supports CDS working mode, which is used to reduce the circuit's KTC noise and FPN noise function; supports (IMRO) working mode. In the CDS mode, the reference signal and the integral signal are read out sequentially, and the frame frequency of the corresponding circuit is reduced by half. The system subtracts the related noise of KTC and FPN by means of quantization and subtraction.

The input stage adopts an improved CTIA structure and supports a linear readout working mode. The linear readout mode is aimed at amplifying small signals with low background. By configuring different three-stage integrating capacitors for

charge-voltage gain conversion, optical signal amplification can be realized. The output supports two-channel, four-channel and eight-channel output modes.

Provide programmable window configuration, image mirroring and flipping functions. The maximum rate of pixel data output is 18Mpixel/sec, and the maximum working frame rate is 300Hz (eight-channel full array 640×512). The circuit supports the application of the shortest integration time of 3 clock cycles. The processing circuit supports three fixed format output (640×512, 640×480, 512×512) and programmable window configuration, and supports serial port operation. The configuration of specific functions and features can be realized by configuring the serial port registers.

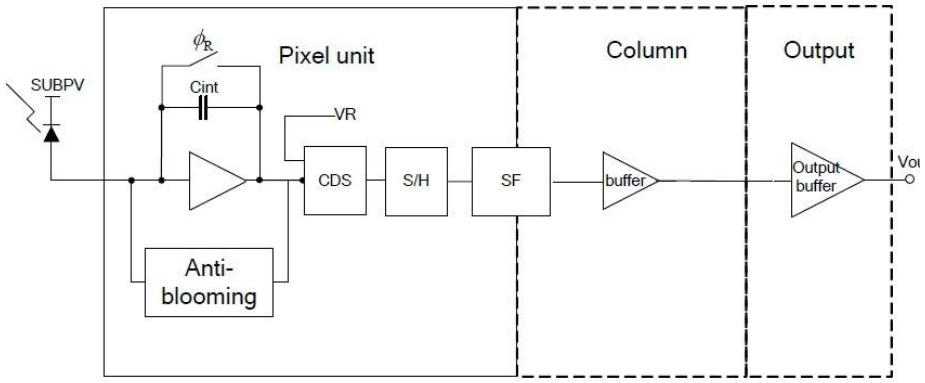


Figure 3. processing circuit structure

6. Working time sequence

According to the user's configuration of different integration signal INT working time sequence, the processing chip automatically enters the working state of ITR (integration-then-reading) or IWR (integration-while-reading).

The pixel unit signal is integrated during the high level period of the integral signal INT, and the analog signal starts to be output after a Thold time has elapsed after the falling edge of the INT. The detailed description is as follows:

Case 1: ITR mode

The signal readout is performed after the current frame signal integration and before the next frame integration. The pixel integration signal of the current frame is readout line by line. After each line has passed Trd, the next line readout will start

until all pixels in the current frame are read. Integral signal. The time used for each signal readout is a master clock cycle Tmc, and the total readout time calculation formula is Tread=Tmc×H×V/N + Trd×(V-1), where N is the number of output channels and H is the number of columns, V is the number of rows. The working frame period of the system is Tframe>Tread+Tint+Thold.

As shown in Figure 4, the pixel unit signal starts to be read after a Thold time from the falling edge of the integral signal INT. See the timing relationship between the signal DATAVALID, LINE1 and the signal INT, where MC is the main clock signal (period is Tmc), and DATAVALID is each line readouts the valid mark signal, the rising edge indicates the start of the signal readout, the falling edge indicates the end of the readout, LINE1 is the first line readout valid mark signal, INT is the frame integration control signal, and the INT high level width is the actual integration Time Tint, which must be an integer number of Tmc. After the falling edge of the int signal, the DATAVALUE signal becomes high through Thold (= 93tmc) and begins to read out the signal data of the first row and the first column of pixels. After the last column of the first row is output, the DATAVALUE signal becomes low; In the whole frame signal output process, the adjacent row output cycle interval TRD (= 32Tmc), and the duration period length of each high level of DATAVALUE is equal to H/N,repeat the above output action until the whole frame pixel signals are read out.

Case 2: IWR mode

The signal readout time is delayed by one Thold (=93Tmc) from the falling edge of the INT of the current frame, and finishes before the falling edge of the INT of the next frame. The high level width of INT is the actual integration time Tint, which must be an integer of Tmc, and the low level width of INT must be greater than 45Tmc, as shown in Figure 5. Integrating the signal in the current frame, and output the analog signal of the previous frame sample-and-hold at the same time to realize the integration-simultaneous-readout function. The time used for each signal readout is a master clock cycle Tmc, and the total readout time calculation formula is Tread=Tmc×H×V/N+Trd×(V-1). In this working mode, the integration time and output time almost overlap, the frame period is approximately equal to the read time, and the system frame period is Tframe>Tread+Thold+320Tmc.After the falling edge of the INT signal, DATAVALUE signal becomes high through Thold (= 93Tmc) and

begins to read out the signal data of the first row and the first column of pixels. After the last column of the first row is output, DATAVALUE signal becomes low; In the whole frame signal output process, the adjacent row output cycle interval Trd (=32Tmc), and the duration period length of each high level of DATAVALUE is equal to H/N. repeat the above output action until the whole frame pixel signals are read out.

Case 3: NDRO mode

As shown in Figure 6, the circuit integrates normally each frame. When NDRO mode is enabled, the circuit outputs the signal data of the frame before NDRO becomes high until it exits NDRO mode, and the circuit outputs the data of the current frame.

Case 4: IMRO mode

As shown in Figure 7, when the IMRO mode is enabled, the internal circuit maintains the integration state, and the signal sampling and readout operations are also performed synchronously according to the frame period of each INT. When the IMRO mode is exited, the internal circuit resumes the integration in the normal frame period-Read the status.

This chip supports serial port configuration internal register status, the action sequence is shown in Figure 8. If the serial port input window is correct, ERROR will go low; otherwise, ERROR will always be high. After the serial port input ends, the register will update the state at the falling edge of the next frame of INT.

When the chip is working, the rising and falling edges of the input clock MC and INT need to meet a certain relationship. As shown in Figure 9, the rising and falling edges of INT are both behind the falling edge of MC (typically 10ns), but the delay time can not exceed the time width of 0.25 master clock MC at most.

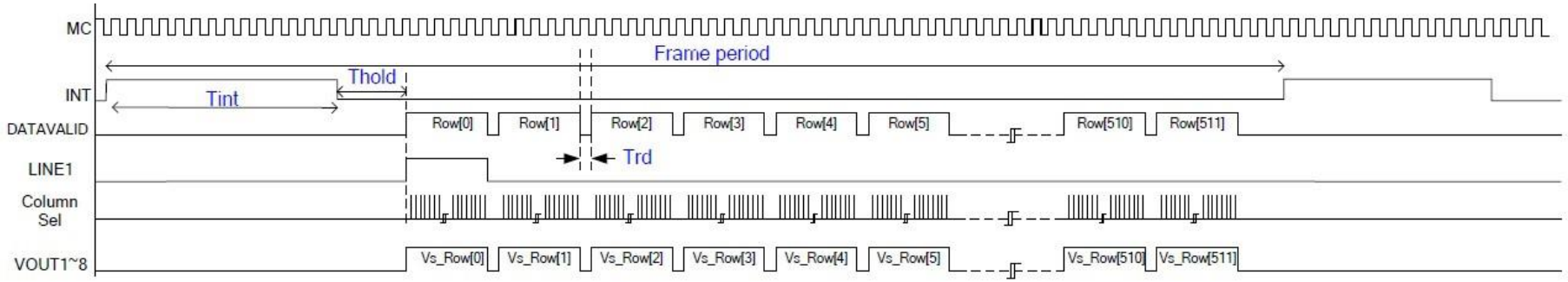


Figure 4. ITR working time sequence diagram

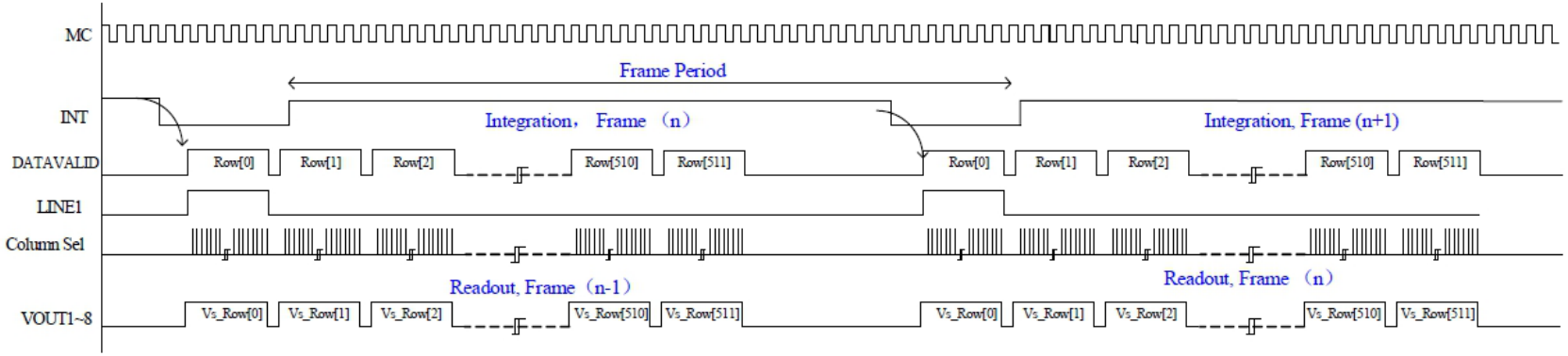


Figure 5. IWR working time sequence diagram

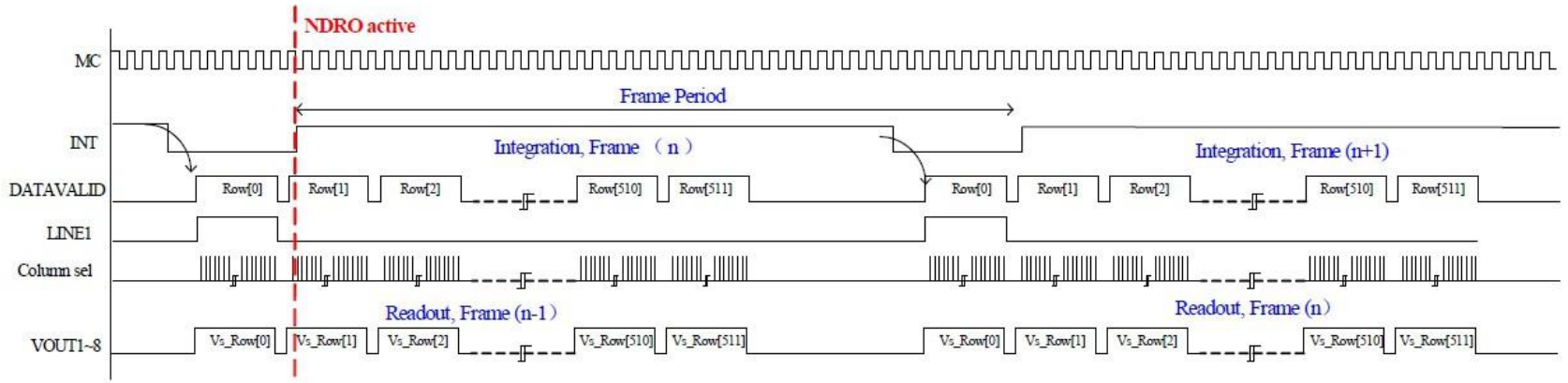


Figure 6. NDRO working time sequence diagram

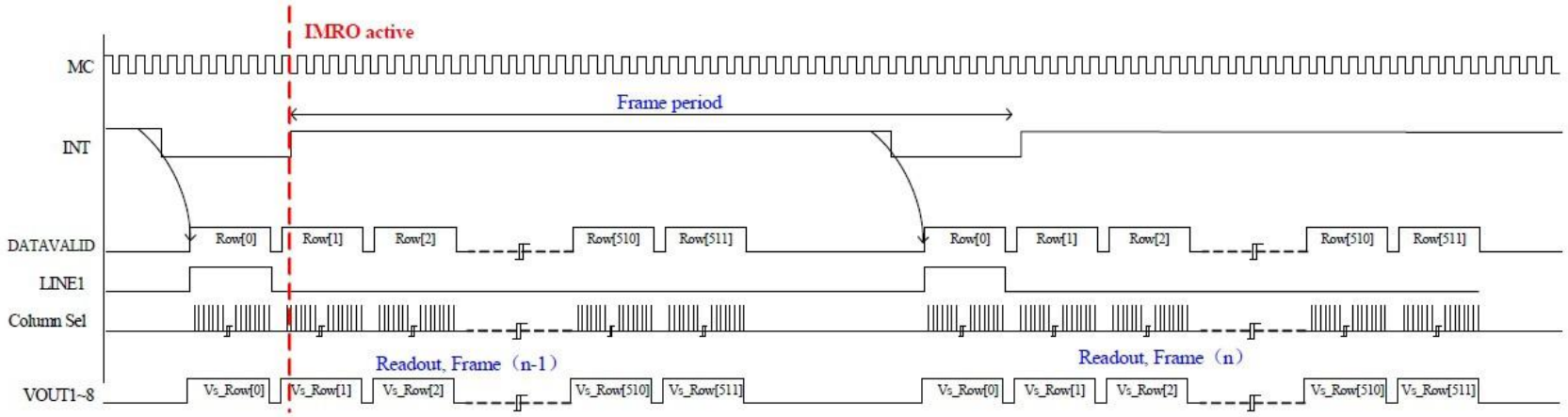


Figure 7.IMRO working sequence diagram

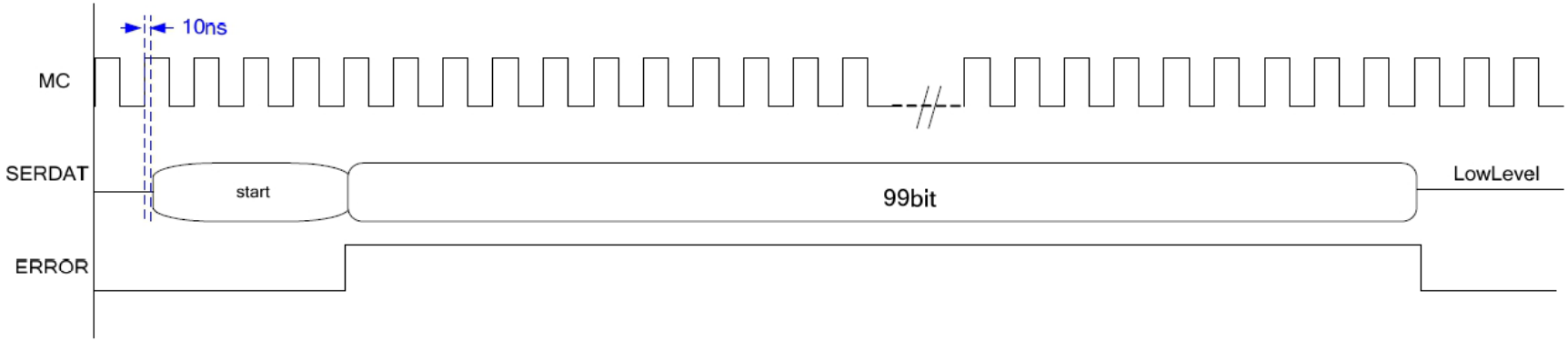


Figure 8. Timing diagram of global serial port register configuration

Note：

1) After the serial port is input, the internal register status is updated at the falling edge of INT in the next frame;

2) The ERROR signal becomes High at the first MC rising edge after the serial port START signal arrives; after the serial port data is read, it becomes .

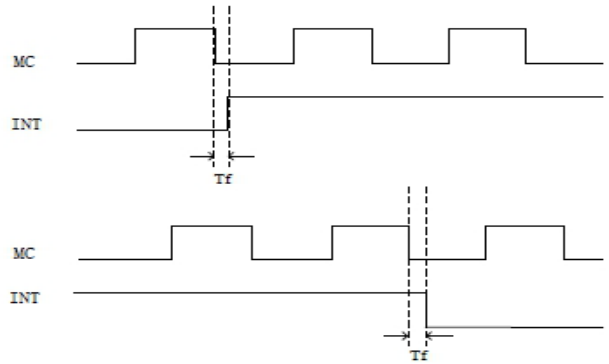


Figure 9. Timing diagram of MC and INT

7． Package parts

7.1 TEC Cooler

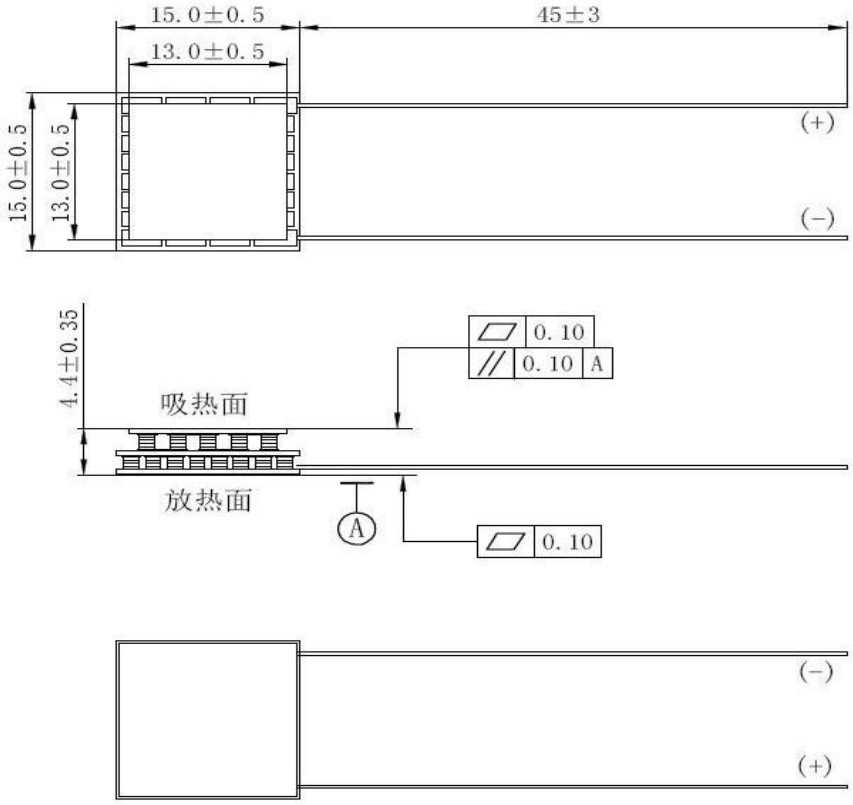


Fig. 10. Outline dimension drawing of TEC cooler

TEC cooler provides the detector with a low-temperature and constant-temperature working environment required for its best performance. The resistance value of TEC is 0.669-0.812Ω (25℃), the maximum current value is 4A, the maximum terminal voltage is 4.2V, the maximum temperature difference is 106.7℃, and the maximum heat absorption is ≥4W.

7.2 Metal shell

The metal shell provides installation and connection standards for optical window systems, detectors, TEC coolers, getter installations, etc., protects the detectors and realizes electrical connections, maintains the vacuum insulation required for the cryogenic and constant temperature operation of the cooler, and

ensures the stable operation of the detectors in the set environment.

7.3 Optical window

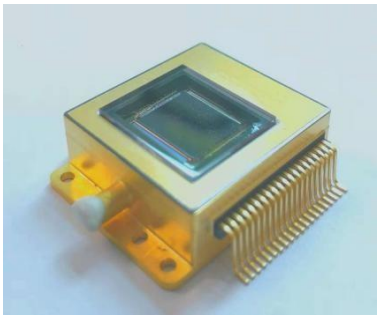


Figure 11. packaging sample

The optical window is made of sapphire or quartz, with a thickness of 1mm. The coating can be designed as needed to limit the transmission wavelength range and adjust the transmission uniformity. The optical window is located at the front end of the metal shell, facing the detector chip, and is relatively fixed in position with the detector chip.

The optical window is a part of the closed vacuum system; At the same time, it also becomes the boundary between the external optical system and the detector chip.

7.4 Vacuum assurance

The detector assembly has been exhausted for a long time with ultra-high vacuum to ensure the long-term vacuum degree of the metal shell. A getter that can be repeatedly activated is also integrated in the component, and the service life of the detector component can be effectively prolonged by activating the getter when the vacuum of the tube shell becomes bad.

8. Product matching and its cross-linking interface relationship

8.1 Supporting status

A complete set of shortwave infrared 640×512 detector unit components is shown in Table 6.

Table 6 short wave infrared 640×Full set of 512 FPA detector unit

Name	Specification	Quantity
Detector assembly	640 × 512/15	1
Product packaging box	——	1
Test report	——	1
User manual	——	1

8.2 Interface

8.2.1 Outline dimension drawing

Refer to figure 1 for the mechanical interface diagram of the 640×512 detector assembly.

8.2.2 Optical interface

optical interface refers to the installation interface between components and optical system, as shown in Figure 2.

8.2.3 Electrical interface

The electronic connection interface mainly includes the metal lead interface of the detector assembly and the vacuum activation electrode.

9. Restrictions and precautions in use and maintenance of the product

9.1 Use and maintenance

9.1.1 Use and operation of components

The operator should wear anti-static gloves or an anti-static wristband and perform the following procedures:

a) Open the detector assembly packaging box and take out the detector assembly (Note: do not touch the lead wire and the sealing part of the exhaust pipe);

b) Connect the lead wire of the detector assembly to the circuit board and apply thermal conductive silicone grease at the bottom, check whether the corresponding electrical connection is correct, and fix it correctly as required to prevent the electrical connection from being disconnected or short-circuited by

vibration;

c) Turn on the TEC refrigeration starting power supply, wait for the temperature sensor indication to reach the detector working temperature, power on and turn on the detector.

9.1.2 Getter activation

a) Getter activation is the normal maintenance of the vacuum system of the component, and the period between two activations should be determined according to the user's actual use of the environment;

b) The getter activation electrodes are located on the pins on both sides of the top of the metal package shell, and connect to a group of getters inside the shell.

9.1.3 Maintenance

The component is a high-tech comprehensive product. Do not handle it by yourself when there is a difficult fault. You should consult the relevant technical personnel or the after-sales service department of the manufacturer for handling advice in time. The component is in a closed state in the application system, except for the professionals to determine the need for vacuum activation, no other daily maintenance is required.

9.2 Trouble Solve

9.2.1 Safety protection device and accident treatment

If any abnormal sound or phenomenon is found during use, stop using it immediately.

9.2.2 Fault analysis and elimination

When a component fails in use, the fault phenomenon should be recorded in time and the cause of the fault should be analyzed.

9.3 Note

a) The detector assembly is a device with high-sensitivity integrated circuit, which must be handled with care to avoid collision. Users should read the technical manual and relevant technical documents in detail before use, and need to receive special technical training;

b) The use of detector components must be equipped with peripheral circuits such as drive circuits and corresponding power supply. The drive circuit includes a dedicated interface circuit that matches the chip circuit interface of the detector component and a low-noise signal adapter circuit.

9.4 Packaging and transportation

a) The product should be transported in a firm packaging box and transported in a prescribed manner;

b) Avoid direct rain and snow and mechanical collision during transportation;

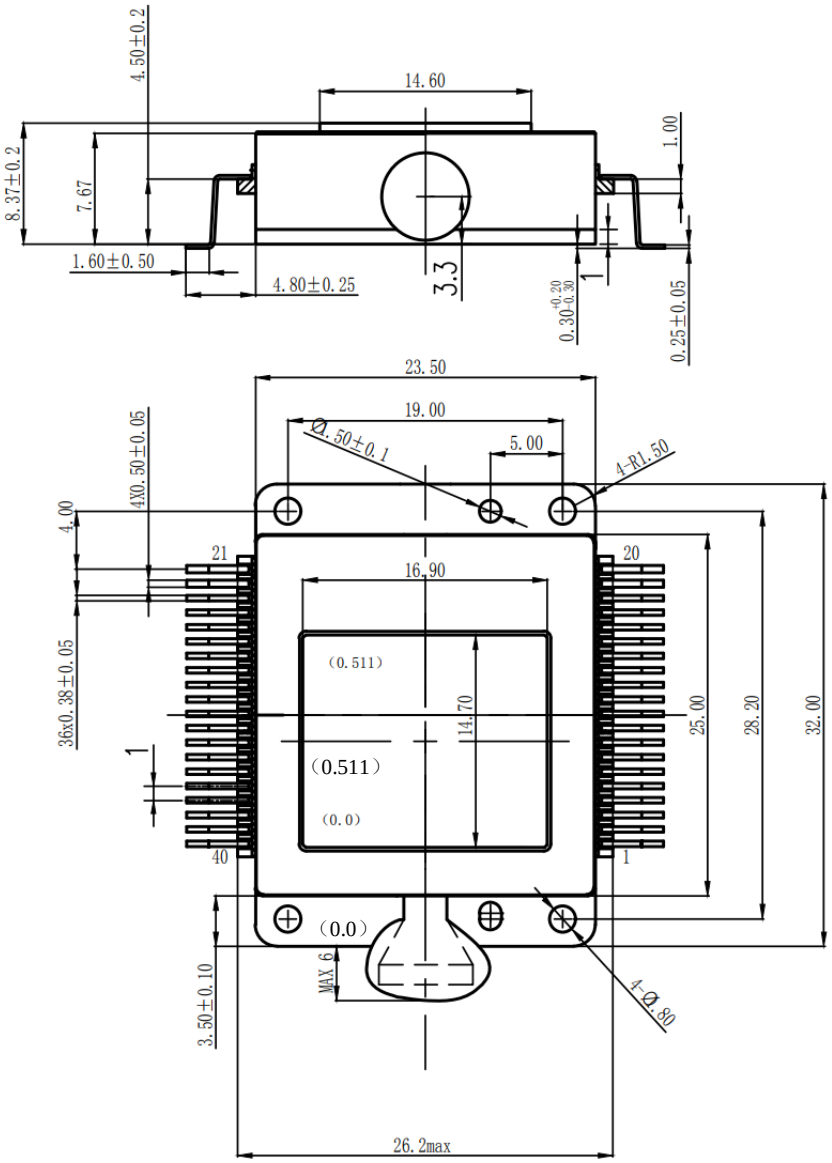
c) Use reliable special packaging and store it properly;

d) The temperature of the storage environment should be kept at −40℃ ~70℃, ventilated, dry and free of corrosive gas.

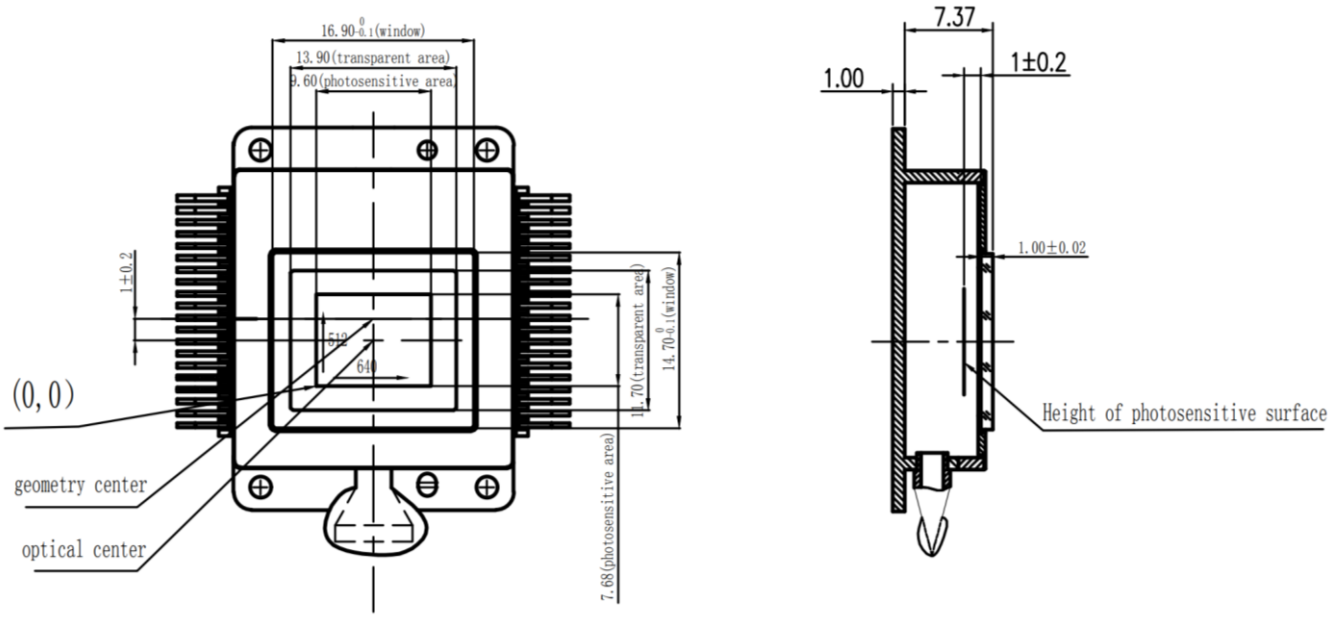
10. Attached figures

Attached Figure 1: Mechanical interface diagram of the detector assembly

Attached Figure 2: Optical interface diagram of the detector assembly



Attached figure 1. Mechanical interface diagram of the detector assembly



Attached figure 2. The position of the optical center of the cover plate and the window of the detector assembly